FIG. 1

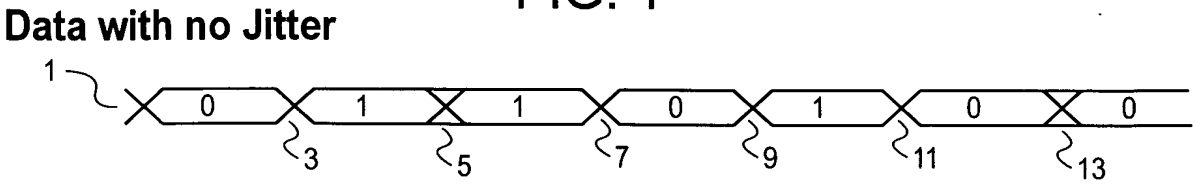


FIG. 2

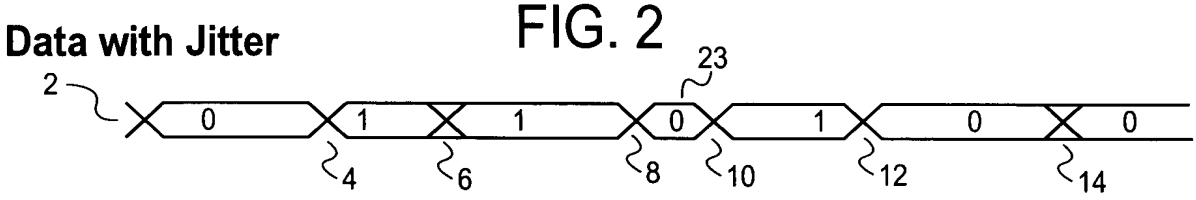


FIG. 3

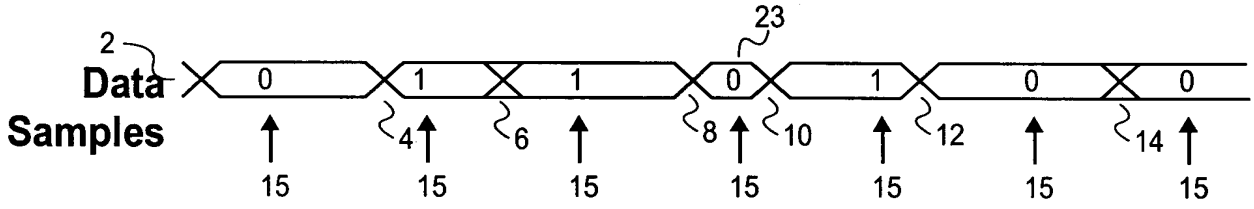
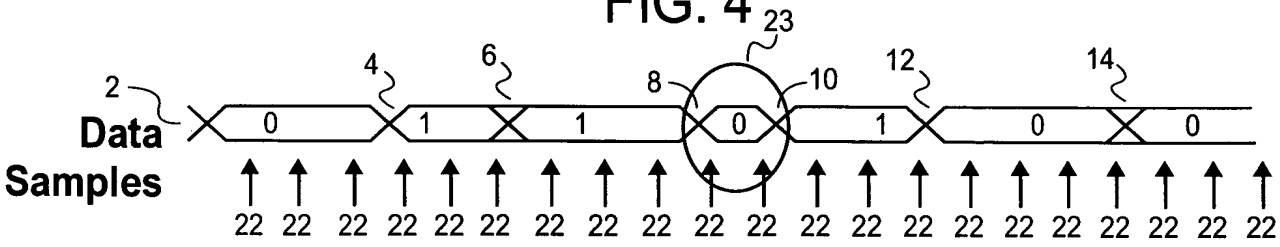
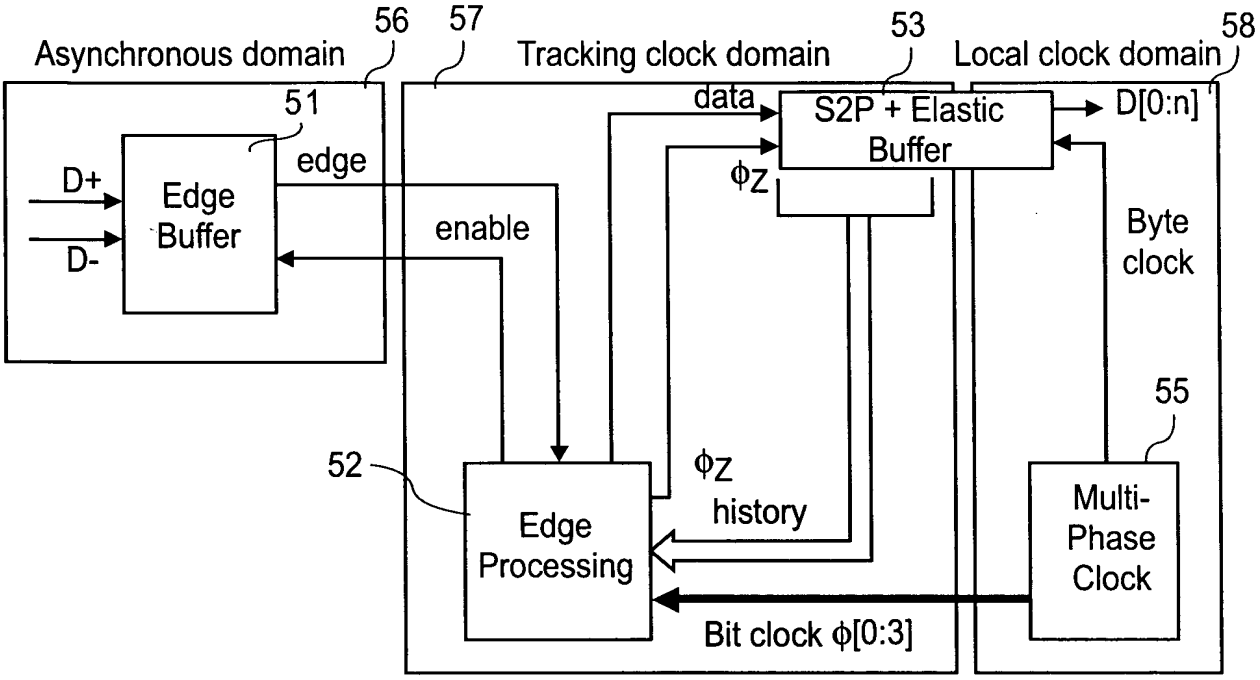


FIG. 4

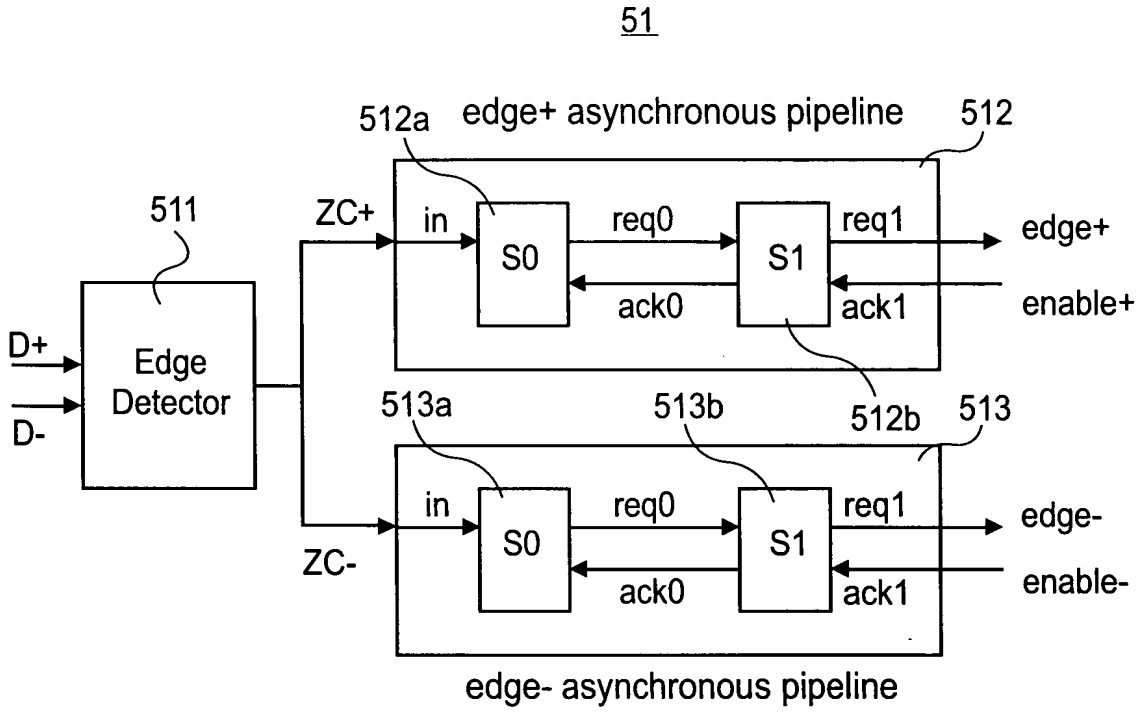


50



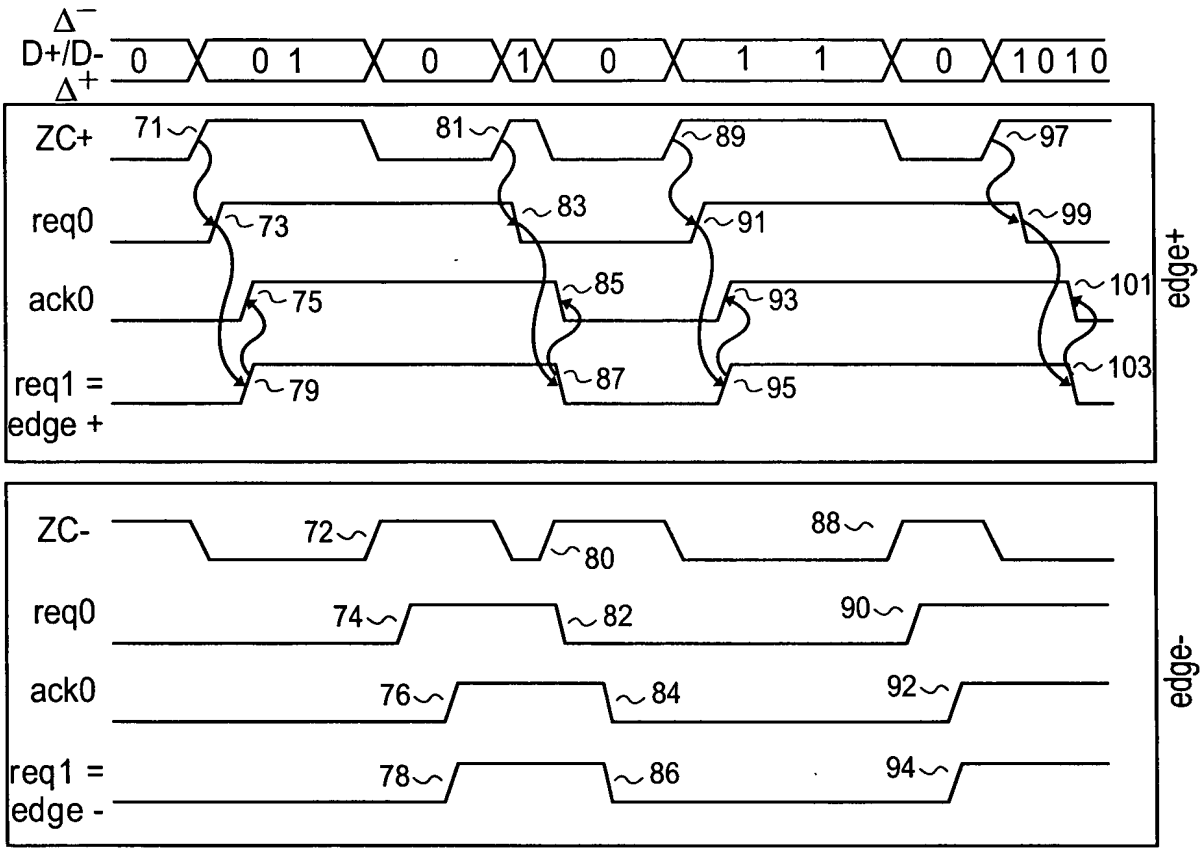
High Level Block Diagram of Edge Based Receiver

FIG. 5



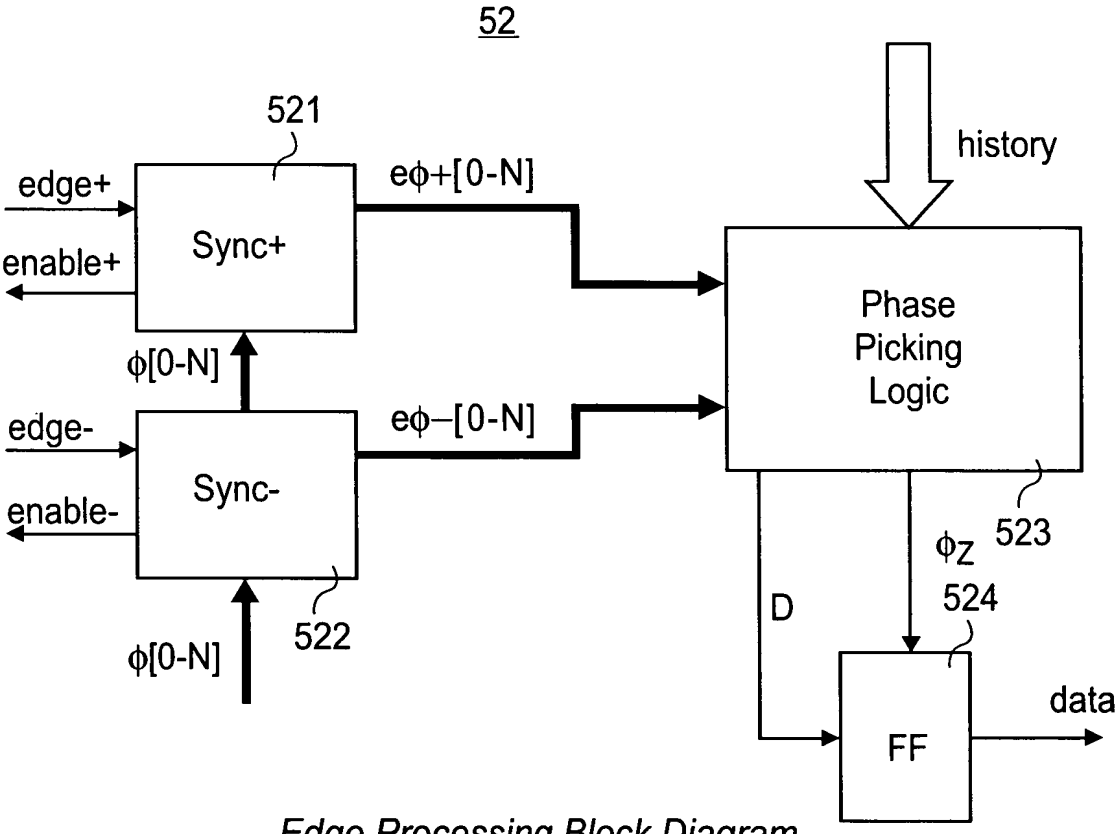
Edge Buffer Block Diagram

FIG. 6



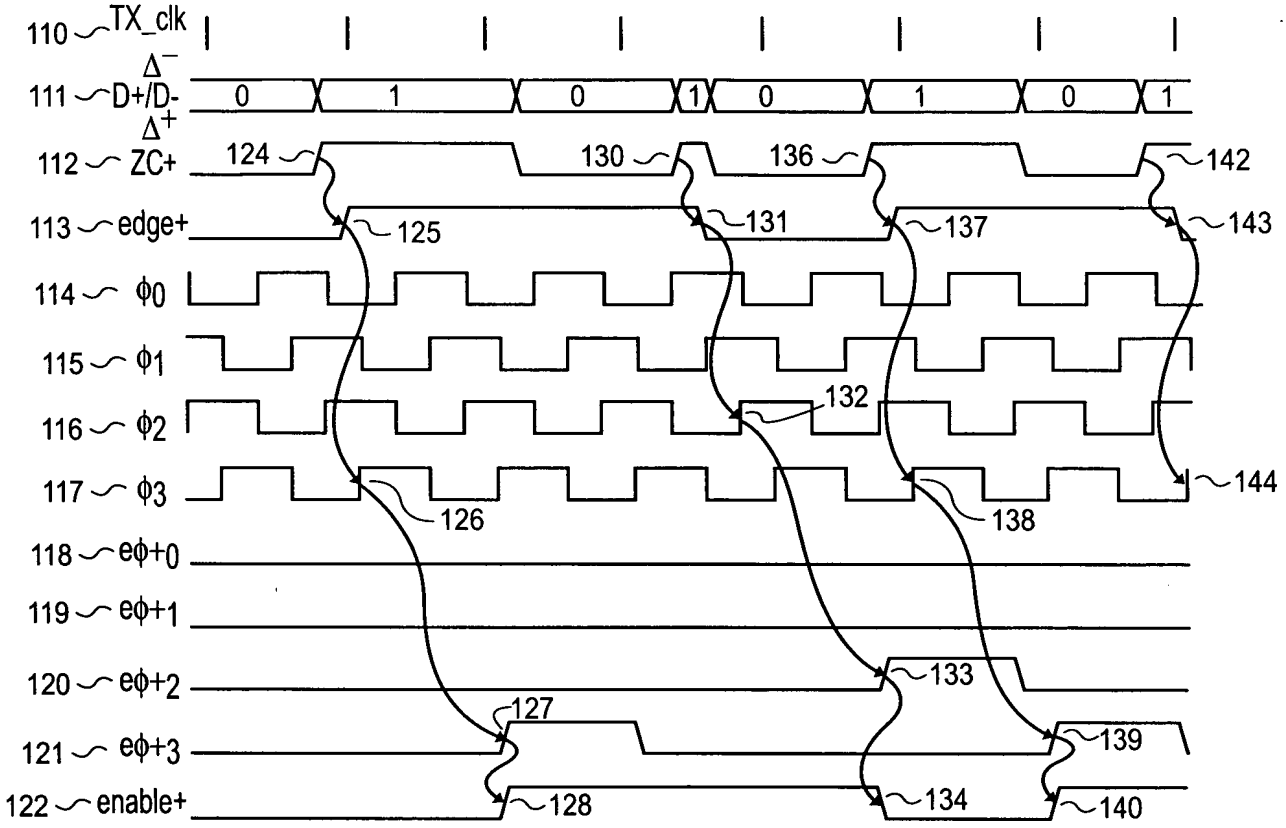
Timing Diagrams for the Edge Pipelines

FIG. 7



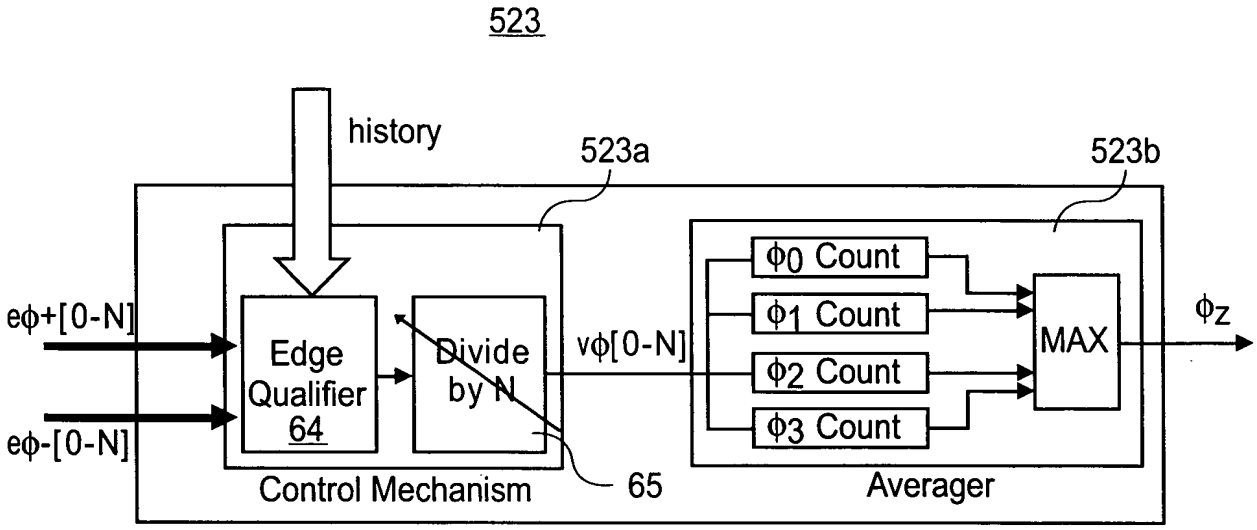
Edge Processing Block Diagram

FIG. 8



Synchronizer Timing Diagram

FIG. 9



Phase Picking Mechanism Block Diagram

FIG. 10

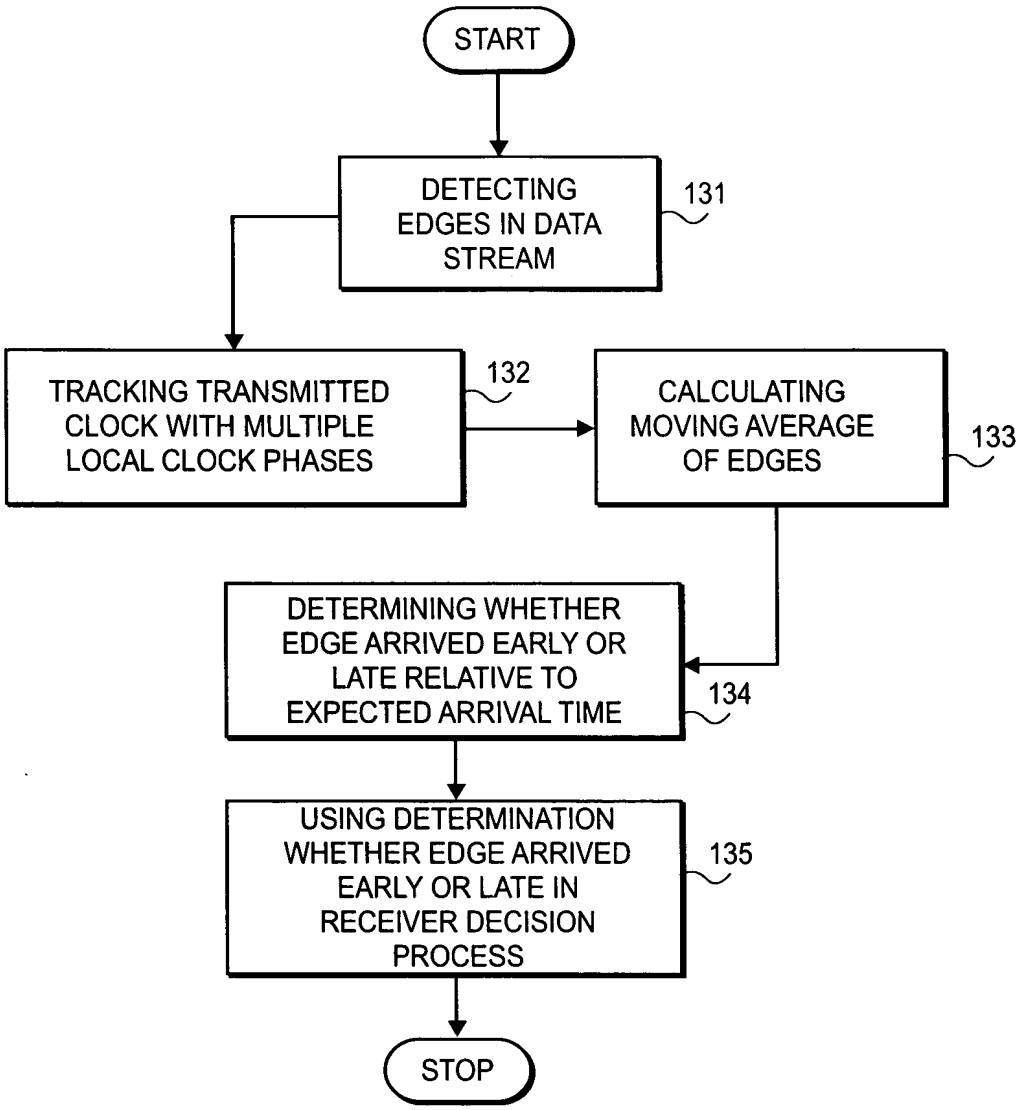

START
DETECTING EDGES IN DATA STREAM
131
TRACKING TRANSMITTED CLOCK WITH MULTIPLE LOCAL CLOCK PHASES
132
CALCULATING MOVING AVERAGE OF EDGES
133
DETERMINING WHETHER EDGE ARRIVED EARLY OR LATE RELATIVE TO EXPECTED ARRIVAL TIME
134
USING DETERMINATION WHETHER EDGE ARRIVED EARLY OR LATE IN RECEIVER DECISION PROCESS
135
STOP
130

FIG. 11

FIG. 12A

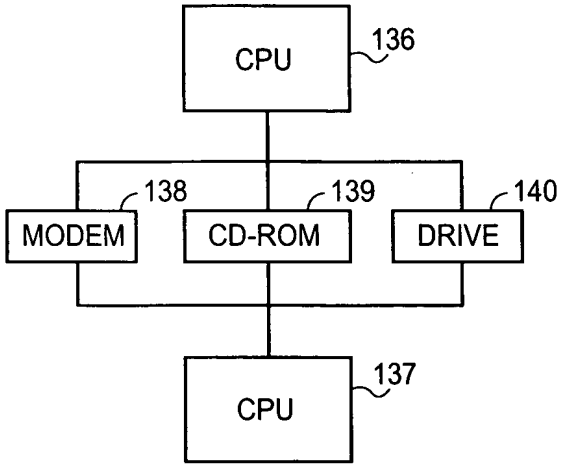


FIG. 12B

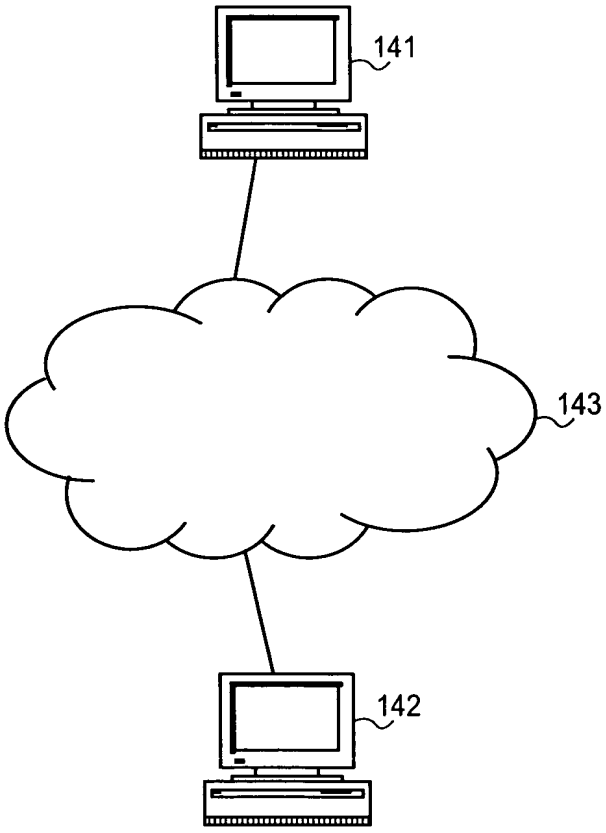


FIG. 12C

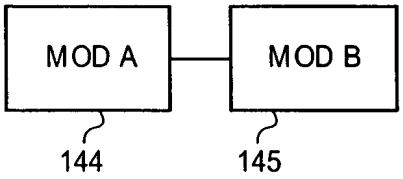
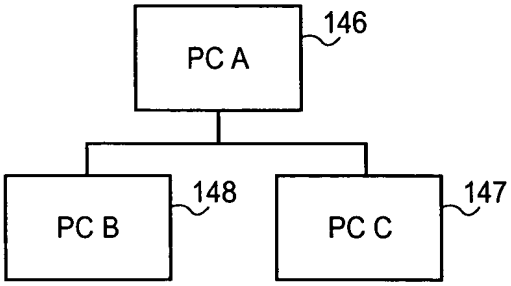


FIG. 12D



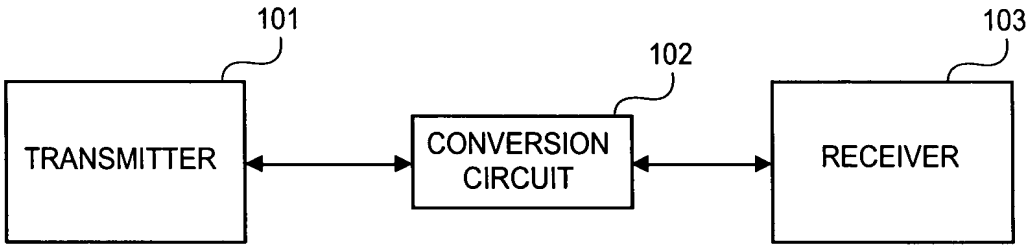


FIG. 13

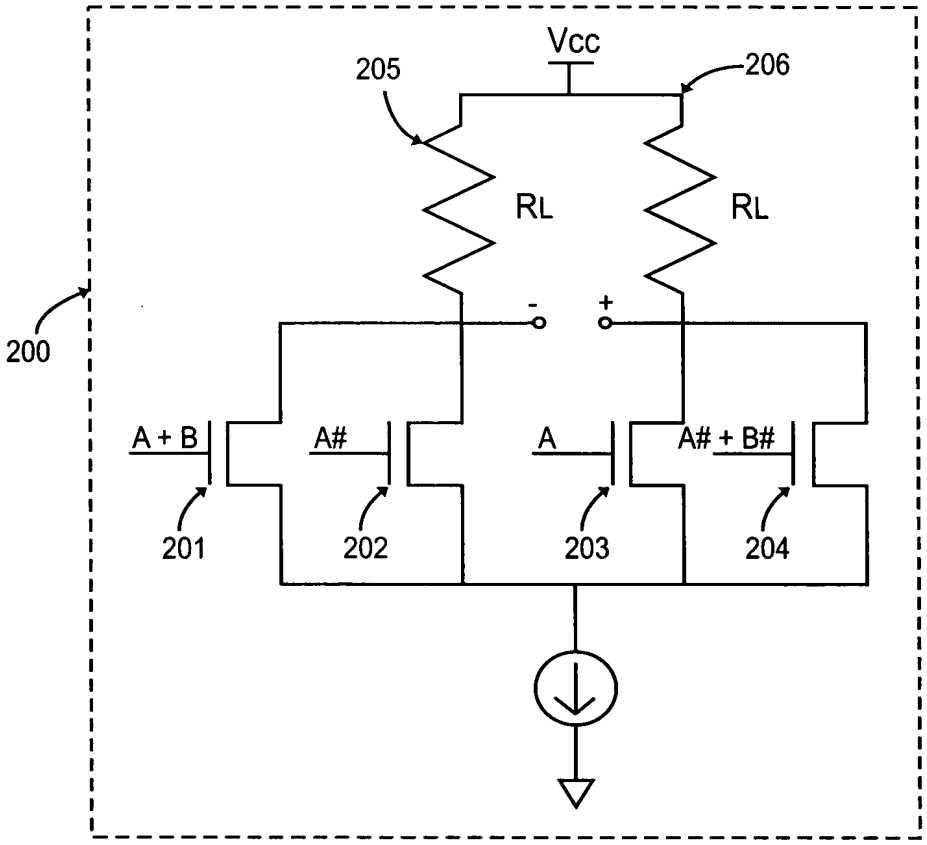


FIG. 14

Signals	A	A#	B	B#	A + B	A# + B#	High Out
Actual Volt.	1.0V	0.5V	0.25V	-0.25V	1.25V	0.25V	+
			-0.25V	0.25V	0.75V	0.75V	-
			0.05V	-0.05V	1.05V	0.45V	+
			-0.05V	0.05V	0.95V	0.55V	-
			0V	0V	1.0V	0.5V	tie
	0.5v	1.0v	0.25V	-0.25V	0.75V	0.75V	+
			-0.25V	0.25V	0.25V	1.25V	-
			0.05V	-0.05V	0.55V	0.95V	+
			-0.05V	0.05V	0.45V	1.05V	-
			0V	0V	0.5V	1.0V	tie

FIG. 15

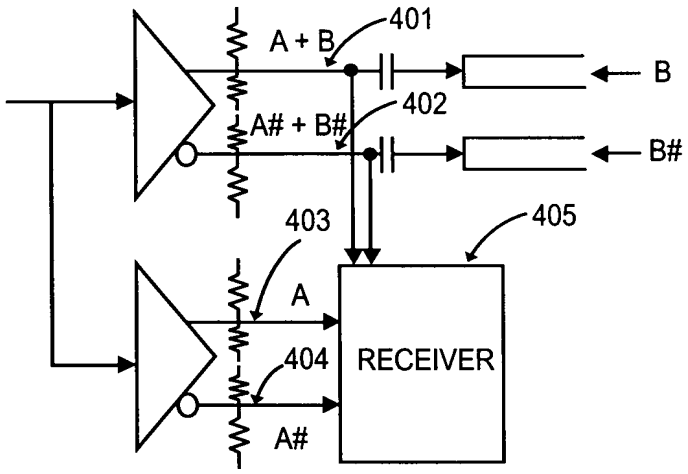


FIG. 16